

ESDLIN1524BJ

TRANSIL™ diode for ESD protection

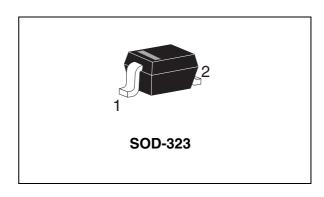
Features

- Max peak pulse power 160 W (8/20 µs)
- Asymmetrical bidirectional device
- Stand-off voltage: 15 and 24 V
- Low clamping factor V_{CL}/V_{BR}
- Complies with the following standards:
 - IEC 61000-4-2 level 4 (> 15 kV air discharge, > 8 kV contact discharge)
 - IEC 61000-4-5; I_{pp} = 3 A (8/20 μ s)
 - HBM MIL STD 833, class 3 (> 4 kV)
- Low Leakage current

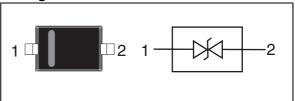
Description

The ESDLIN1524BJ is an asymmetrical TRANSIL diode designed specifically for protecting one automotive LIN bus line against electrostatic discharge (ESD). The SOD-323 is a very small package which allows space saving on high density printed circuit board .

Transil diodes provide high overvoltage protection by clamping action and have instantaneous response to transient overvoltages.



Configuration



Pin	Description					
1	Cathode 1 (15 V reverse stand-off voltage)					
2	Cathode 2 (24 V reverse stand-off voltage)					

Table 1. Absolute maximum ratings (limiting values) $T_{amb} = 25^{\circ} C$

Symbol	Parameter	Value	Unit	
P _{PP}	Peak pulse power dissipation 8/20 µs (1)	T_j initial = T_{amb}	160	W
T _{stg} T _j	Storage temperature range Operating junction temperature range		-65 to +175 -40 to 150	° C
T _L	Maximum lead temperature for soldering during 10 s		260	° C

^{1.} For a surge greater than maximum values, the diode will fail in short-circuit

Table 2. ESD Maximum ratings

Symbol	Parameter	Conditions	Value	Unit
ESD Electrostatic discharge capability		IEC 61000-4-2 (contact discharge)		
ESD	Electrostatic discharge capability	HBM MIL STD 833	10	kV

TM: TRANSIL is a trademark of STMicroelectronics.

Characteristics ESDLIN1524BJ

1 Characteristics

Table 3. Electrical characteristics $(T_{amb} = 25^{\circ} C)$

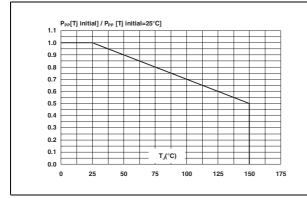
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Symbol	Parameter	ΙΑ
V _{RM}	Stand-off voltage	Ţ _p
V_{BR}	Breakdown voltage	
V _{CL}	Clamping voltage	I I
I _{RM}	Leakage current @ V _{RM}	$V_{\mathrm{CL}}V_{\mathrm{BR}}$ V_{RM} I_{RM} I_{RM} V_{RM} V_{CL}
I _R	Breakdown current @ V _{BR}	Į k
I _{PP}	Peak pulse current	
С	Junction capacitance	

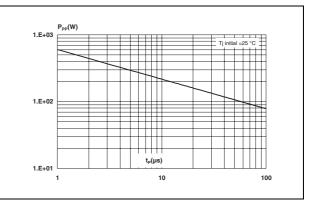
	I _{RM} @V _{RM}			V _{BR} @ I _R ⁽¹⁾			V _{CL max} @ I _{PP} 8/20 μs				C ⁽²⁾		α T (3)	
Types	nA V		V		mA	v	Α	v	Α	pF		10 ⁻⁴ /°C		
	Тур	Max		Min	Тур	Max	IIIA	•	_	•	A	Тур	Max	Max
ESDLIN1524BJ(15V)	1	50	15	17.1	18.9	20.3	5	25	1	35	5	16	20	8.8
ESDLIN1524BJ(24V)	1	50	24	25.4	27.8	30.3	5	40	1	50	3	16	20	9.6

- 1. Pulse test: $t_p < 50 \text{ ms}$
- 2. $V_R = 0 V, F = 1 MHz$
- 3. $\Delta V_{BR} = \alpha T x (T_{amb} -25) x V_{BR(25^{\circ} C)}$

Figure 1. Relative variation of peak pulse power versus initial junction temperature

Figure 2. Peak pulse power versus exponential pulse duration

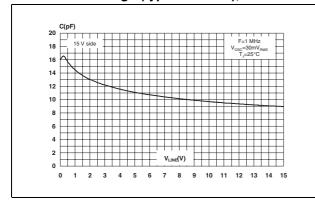


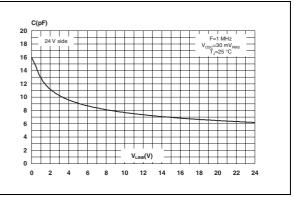


ESDLIN1524BJ **Characteristics**

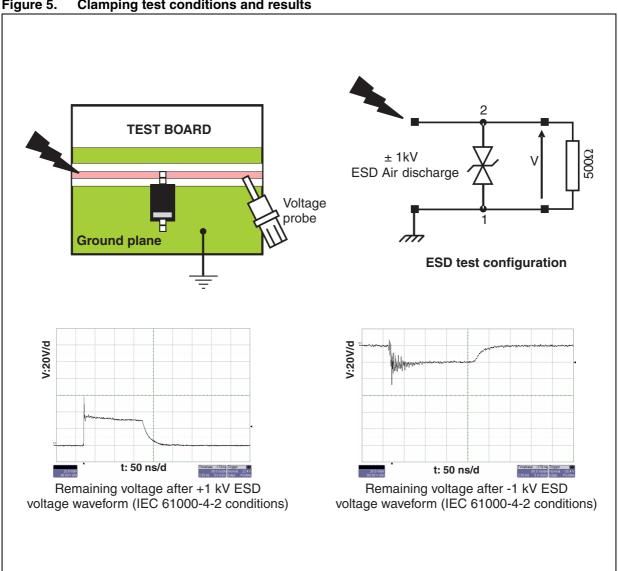
Figure 3. Junction capacitance versus line voltage (typical values), 15 V side

Figure 4. Junction capacitance versus line voltage (typical values), 24 V side





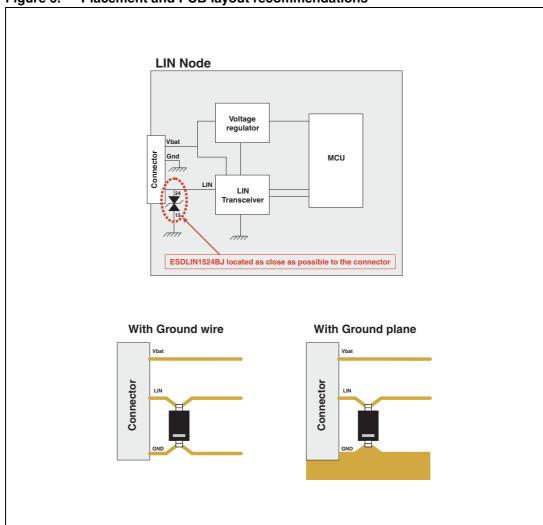
Clamping test conditions and results Figure 5.



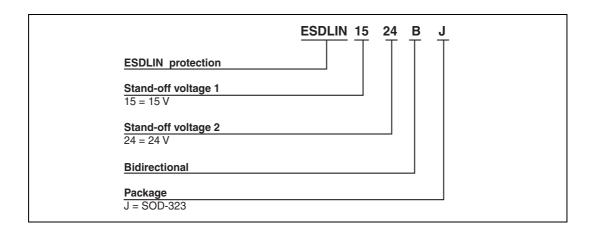
2 Placement and PCB layout recommendations

Figure 6. illustrates recommendations for the placement and layout of the PCB for optimum benefit of the ESDLIN1524BJ.

Figure 6. Placement and PCB layout recommendations

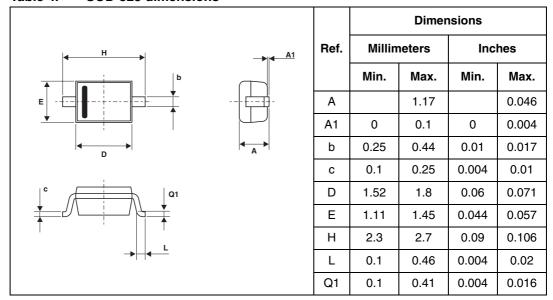


3 Ordering information scheme



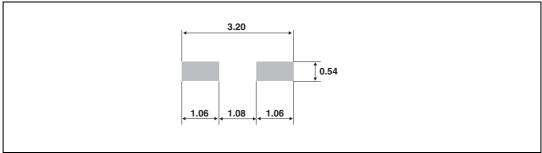
4 Package information

Table 4. SOD-323 dimensions



Ordering information ESDLIN1524BJ

Figure 7. SOD-323 footprint (dimensions in millimeters)



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5 Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDLIN1524BJ	24	SOD-323	5 mg	3000	Tape and reel

6 Revision history

Date	Revision	Changes
28-Aug-2006	1	Initial release.
22-Sep-2006	2	Added Figure 6 Placement and layout recommendations.

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